Texas Instruments

TPS54314 3-A Internally Compensated SWIFT™ Regulator EVM

User's Guide

July 2003

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It is important to operate this EVM within the input voltage range of 3 V to 6 V

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the TPS54314, 3-A, 1.8-V, internally compensated, SWIFT™ regulator evaluation module (EVM). This user's guide includes a schematic diagram and bill of materials.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

Related Documentation From Texas Instruments

- *SWIFT™ Designer* software tool
- Application report SLVA111—*Designing With the TPS54311 Through TPS54316 Synchronous Buck Regulators*

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Contents

Figures

Tables

Chapter 1

Introduction

This chapter contains background information for the TPS54314 and support documentation for the TPS54314 evaluation module. The EVM performance specifications are also given.

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1.1 Background

The TPS54314EVM evaluation module uses the TPS54314 synchronous buck regulator to provide a 1.8-V output over an input range of 3 V to 6 V and over a load range of 0 A to 3 A. The electrical components of the TPS54314 circuit consume less than 0.6 square inches of board space. Additional pads are provided to support multiple input and output capacitors. A jumper is provided to allow the switching frequency to be easily changed from 350 kHz to 550 kHz.

The TPS54314 has two key features that reduce the number of additional components compared to traditional synchronous buck controllers. The first feature is that the MOSFETs are incorporated inside the TPS54314 package. This eliminates the need for external MOSFETs and their associated drivers. The second feature is that the compensation components that stabilize the feedback loop are also incorporated inside the TPS54314 package.

Because the internal compensation of the TPS54314 is fixed, loop stability is assured by the proper selection of an output inductor and output capacitor. For guidelines on selecting an output inductor and output capacitor for a specific application, refer to Texas Instruments application report, literature number SLVA111, *Designing With The TPS54311 Through TPS54316 Synchronous Buck Regulators.*

1.2 Performance Specification Summary

Table 1–1 provides a summary of the TPS54314EVM performance specifications. All specifications are given for an ambient temperature of 25°C, unless otherwise noted.

Table 1–1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		3	5	6	V
Output voltage set point			1.8		V
Output current range		0		3	A
Load regulation	V_I = 5 V	–7		7	mV
Load transient response	I_O = 0 A to 3 A		–60		mV_{PK}
			30		µs
	I_O = 3 A to 0 A		70		mV_{PK}
			30		µs
Loop bandwidth	V_I = 5 V, I_O = 3 A		70		kHz
Phase margin	V_I = 5 V, I_O = 3 A		49		°
Input ripple voltage			150		mV_{PP}
Output ripple voltage			15	30	mV_{PP}
Output rise time		2.6	3.6	4.1	ms
Operating frequency		640	700	760	kHz
Efficiency	V_I = 5 V, I_O = 1 A		91.5%		

1.3 Modifications

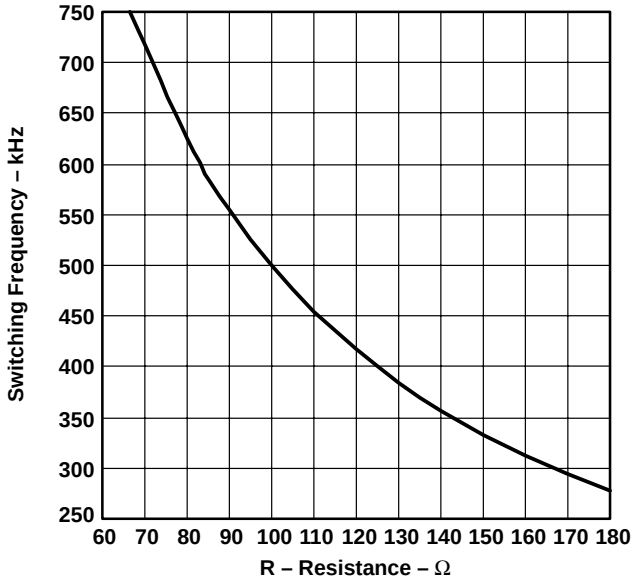
1.3.1 General

The TPS54314EVM is designed to demonstrate the small amount of board space taken up by the TPS54314 electrical components. In addition, the EVM can be used to evaluate different output filters by substituting an alternative inductor for L1, or by using the optional pads for capacitors C2 and C10 (see Figure 4–1). Because the feedback compensation is fixed by the internal circuitry of the TPS54314, proper selection of the output inductor and output capacitor ensures stability. The *SWIFT Designer* software tool or Texas Instruments application note SLVA111 can be used to assist in the selection of an output filter. Both SWIFT Designer and SLVA111 are available for download at the Texas Instruments web site.

1.3.2 Switching Frequency

The TPS54314 is configured to switch at a frequency of 700 kHz. Alternatively the EVM can be easily configured to switch at either 350 kHz or 550 kHz by removing the frequency trimming resistor R3 and placing the shunt on jumper JP1 in the proper location. Also, by changing the value of RT (R3), the switching frequency can be trimmed to any value between 280 kHz and 700 kHz. A plot of the value of RT versus the switching frequency is given in Figure 1–1.

Figure 1–1. Frequency Trimming Resistor Selection Graph



1.3.3 Output Voltage

The EVM can be modified for different preset output voltages by using other devices in the TPS5431x family. The only U1 component needs to be changed. Table 1–2 lists the devices required for U1 for different output voltage options.

Table 1–2. Device Modification

Output Voltage (V)	Device (U1)
0.9	TPS54311
1.2	TPS54312
1.5	TPS54313
1.8	TPS54314
2.5	TPS54315
3.3	TPS54316

1.3.4 Slow Start

The slow start time of the TPS54314EVM can be modified by changing the value of C1. Equation 1 can be used to calculate the value of C1 for a specific slow start time. With C1 left open, the slow start time is typically 3.6 ms. The slow start time can not be made faster than 3.6 ms.

$$C_1 = \frac{T_{SS} \times 5\ \mu A}{0.891\ V} \quad (1)$$

Chapter 2

Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54314EVM. It also presents the test results and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up

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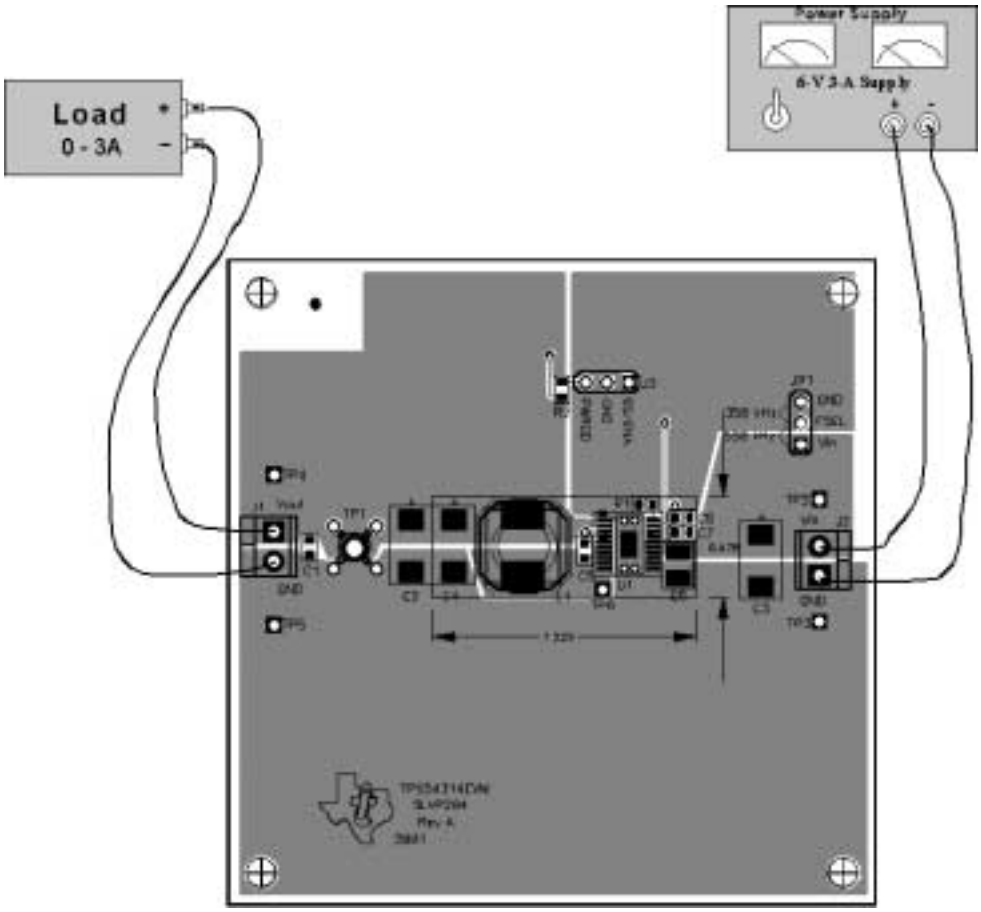
2.1 Input/Output Connections

The TPS54314EVM has the following four input/output connections: J1 (V_I and GND) and J2 (V_O and GND). A diagram showing the connection points is shown in Figure 2–1. Connect a power supply capable of supplying 3 A to J1 through a pair of 20 AWG wires. Connect the load to J2 through a pair of 20 AWG wires. Minimize wire lengths to reduce losses in the wires. Test point TP8 provides easy connection for an oscilloscope voltage probe to monitor the output voltage.

Figure 2–1. Connection Diagram



2.2 Efficiency

The TPS54314EVM efficiency peaks at around 1 A of load current, with a 5-V input source. At full load this drops to around 85%. Figure 2–2 shows the typical efficiency for both a 5-V input and a 3.3-V input and an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is also slightly higher at lower switching frequencies due to the gate and switching losses in the MOSFETs. The efficiency is slightly higher with a 5-V input because the higher input voltage provides more drive voltage for the power MOSFETs, which leads to a lower drain-to-source resistance. The total board losses are shown in Figure 2–3.

Figure 2–2. Measured Efficiency

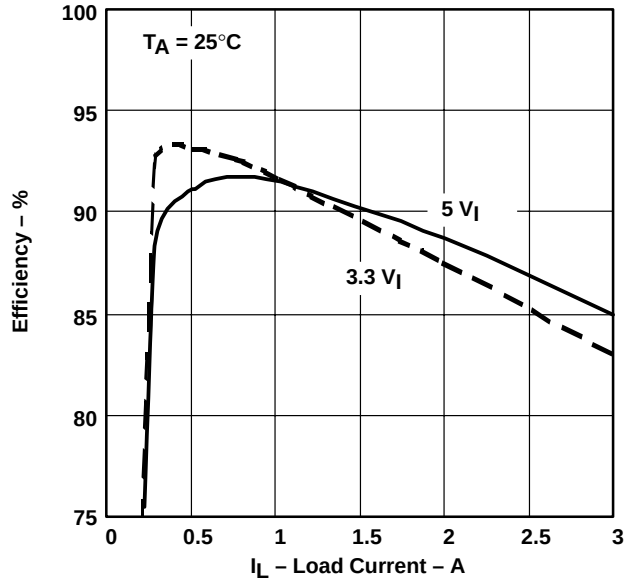
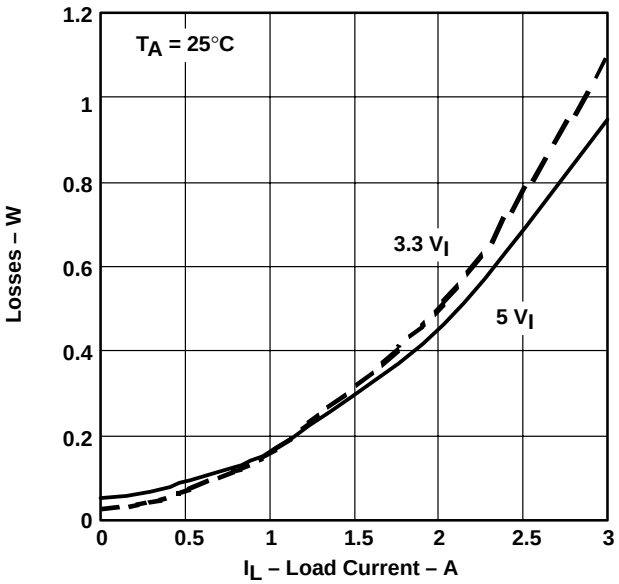


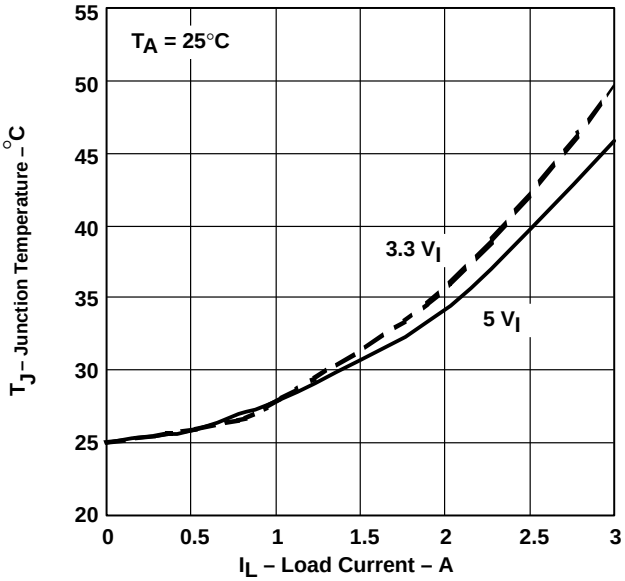
Figure 2–3. Measured Board Losses



2.3 Thermal Performance

The junction temperature is plotted versus the load current with a 25°C ambient temperature in Figure 2–4. The low junction-to-case thermal resistance of the PWP package, along with a good board layout, helps to keep the junction temperature low at high output currents. With a 5-V input source and a 3-A load, the junction temperature is approximately 45°C.

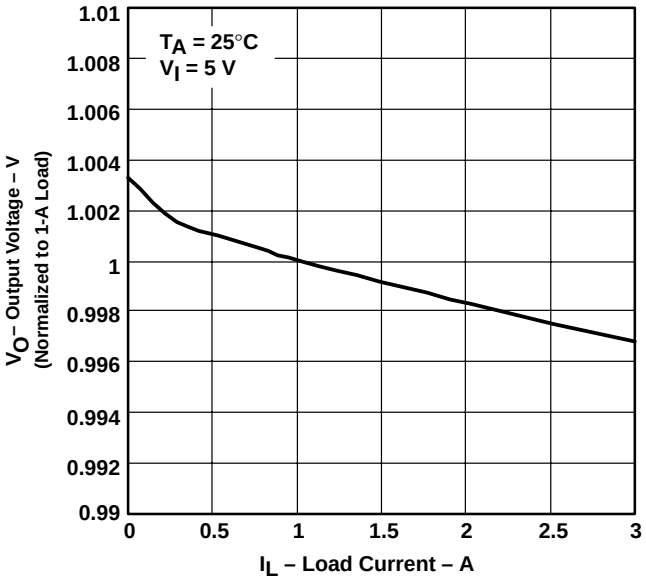
Figure 2–4. Measured Junction Temperature at 25°C Ambient



2.4 Output Voltage Regulation

The output voltage load regulation with a 5-V input and a 25°C ambient temperature is shown in Figure 2–5. Over the load range of 0 A to 3 A, the output voltage varies less than 0.35%.

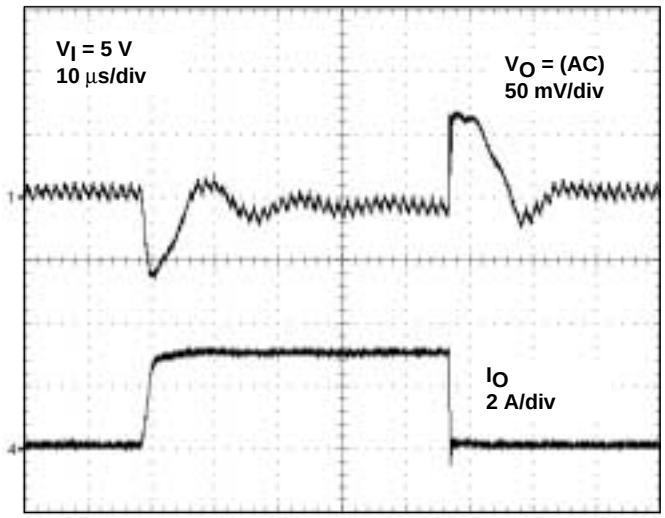
Figure 2–5. Measured Load Regulation



2.5 Load Transients

The TPS54314EVM response to load transients is shown in Figure 2–6. The load transient in Figure 2–6 transitions between 0 A and 3 A. The output voltage deviates approximately –60 mV (–3.3%) and 70 mV (3.9%) from its average value as a result of these transients. In Figure 2–6, the output voltage returns to a ±2% regulation band within 30 μs.

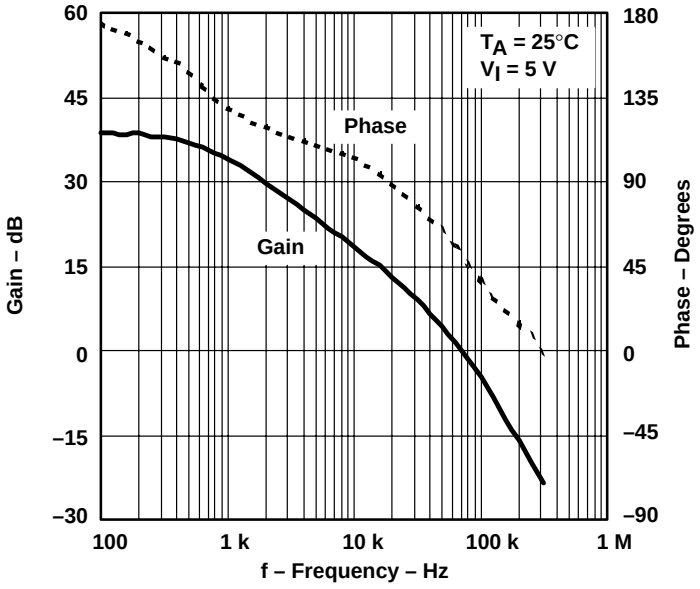
Figure 2–6. Measured Load Transient Response



2.6 Loop Characteristics

The loop gain and phase for a 5-V input and a 3-A load is shown in Figure 2–7. The loop crossover frequency is approximately 70 kHz, and the phase margin is approximately 49°.

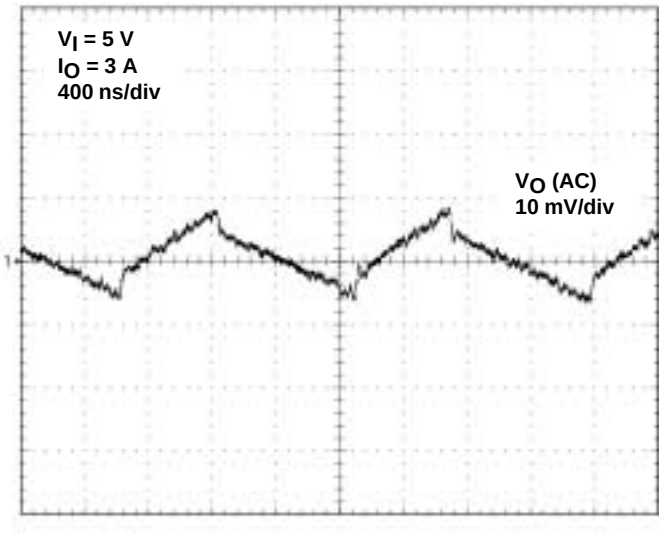
Figure 2–7. Measured Loop Gain and Phase



2.7 Output Ripple Voltage

The output ripple voltage is plotted in Figure 2–8 with an input voltage of 5 V and a load current of 3 A. The TPS54314EVM has a typical output voltage ripple of less than 20 mV_{pp}. If the switching frequency is reduced, the output ripple voltage is higher.

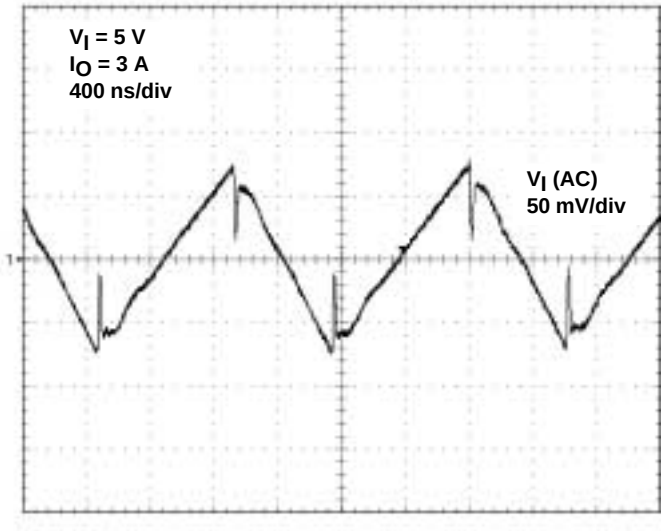
Figure 2–8. Measured Output Ripple Voltage



2.8 Input Ripple Voltage

The input ripple voltage for a 3-A load is shown in Figure 2–9. With an input voltage of 5 V, the input ripple is approximately 150 mV_{pp}. The input ripple voltage can be made lower by adding capacitance to the input.

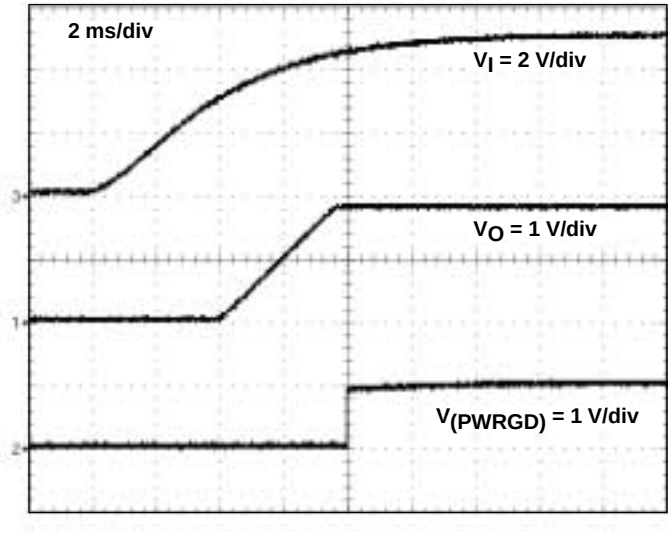
Figure 2–9. Measured Input Ripple Voltage



2.9 Start-Up

The start-up voltage waveform of the TPS54314EVM, with C1 left open, is shown in Figure 2–10. In Figure 2–10, the input voltage is displayed on channel 3, the output voltage is displayed on channel 1, and the power good signal is displayed on channel 2. Once the input voltage rises above the 2.9-V start-up threshold, the output voltage begins to rise linearly to 1.8 V in 3.6 ms. Once the output voltage has reached its final value, the open-drain power good signal rises to a high state. The start-up time can be extended by using an external slow start capacitor, C1. To program a specific slow start time, see section *1.3.4 Slow Start.* The shorting jumper on J2 should not be used to enable the EVM. Using the J2 jumper may cause excessive voltage transients on the SS/ENA pin. Use an external enable signal, instead of J2 jumper.

Figure 2–10. Measured Start-Up Waveforms



Chapter 3

Board Layout

This chapter provides a description of the TPS54314EVM board layout and layer illustrations.

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3.1 Layout

The top-side (component) layer for the TPS54314EVM is shown in Figure 3–1. The input capacitor (C6), bias decoupling capacitor (C7), and bootstrap capacitor (C5) are all located as close to the IC as possible.

The TPS54314EVM PWB consists of two layers of 1.5 oz. copper. The bottom half of the top layer is used as a power ground plane, while the bottom layer is used as a *quiet* (analog) ground plane. A wide power ground plane is used to keep the power ground current from degrading the load regulation. The two ground planes tie together at U1 to keep the ground current from injecting noise between the analog and power grounds. A total of 10 vias are used to tie the thermal land area under the TPS54314 device to the thermal plane on the backside of the board.

Figure 3–1. Top Side Assembly

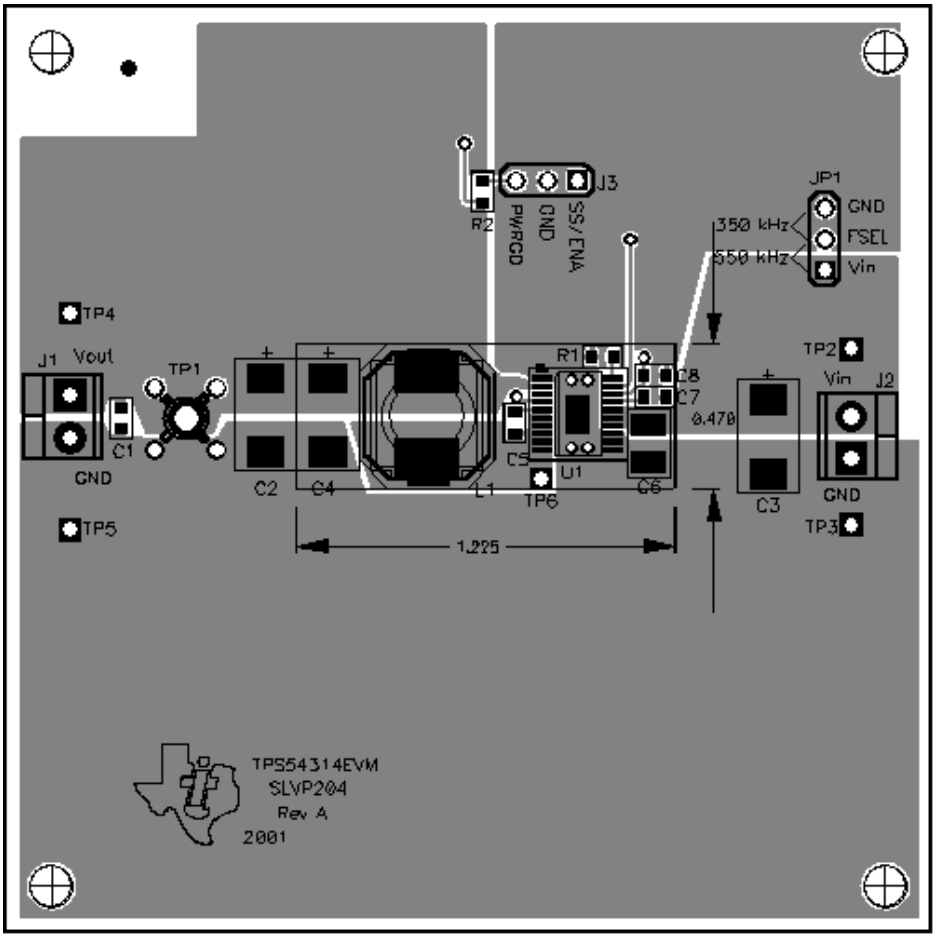


Figure 3–2. Top Side Layout

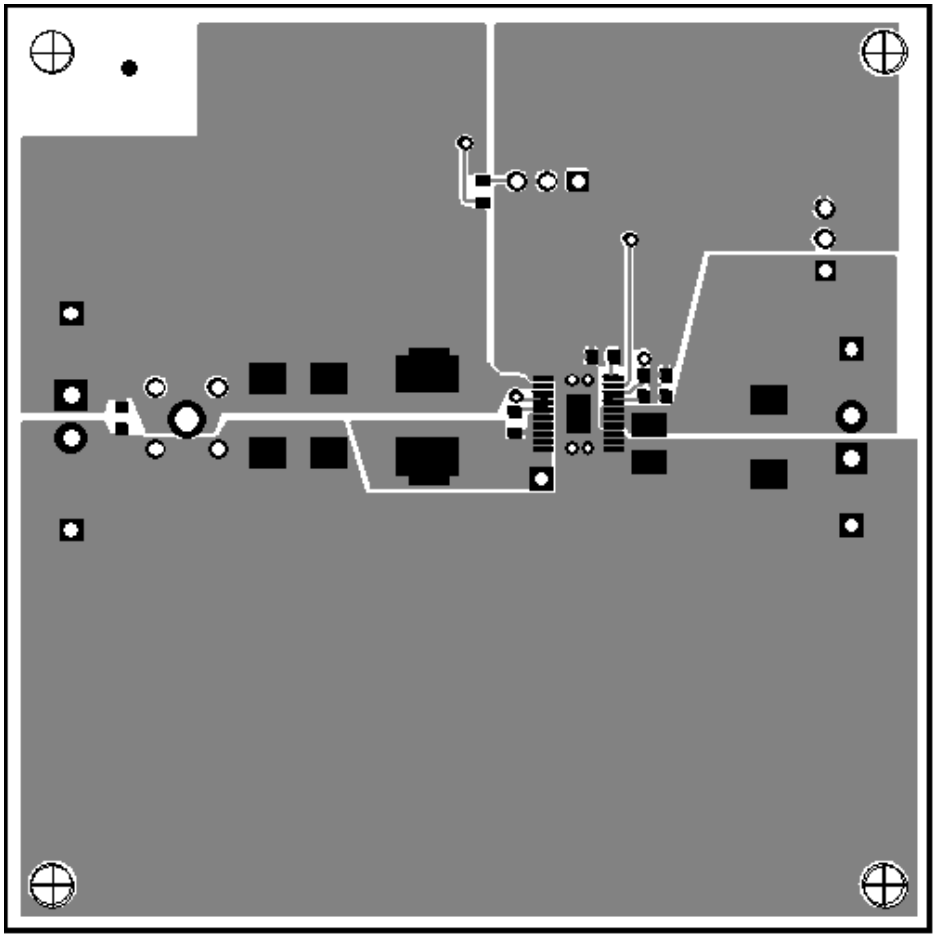
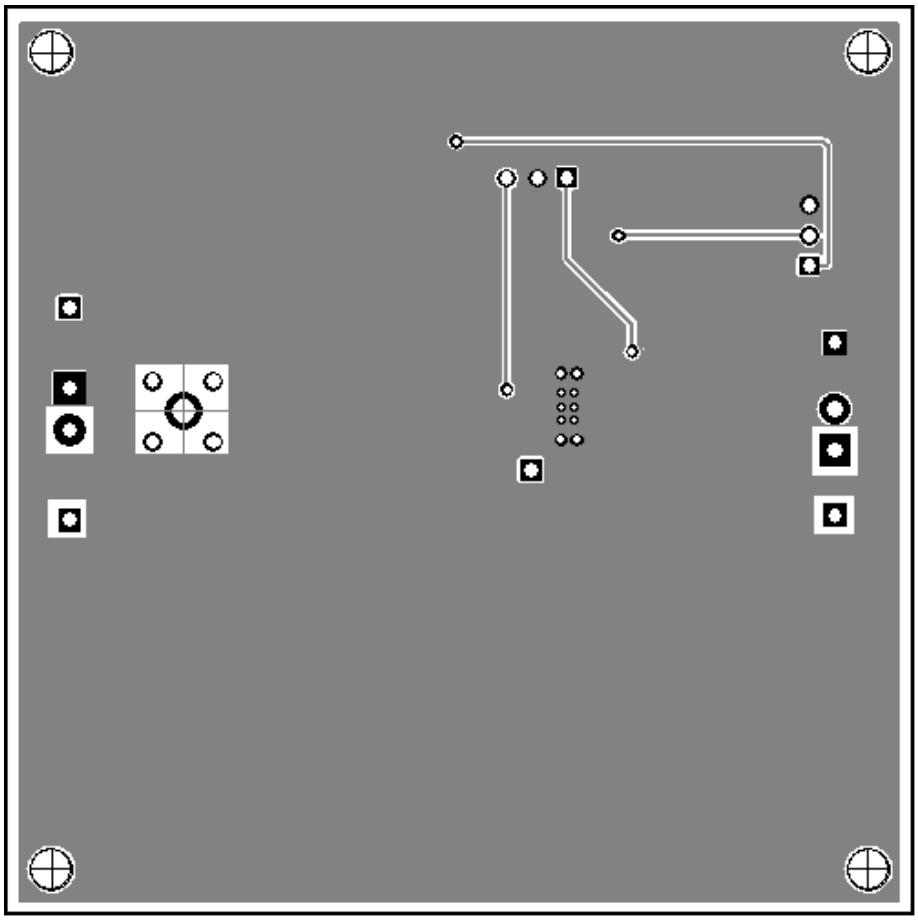


Figure 3–3. Bottom Side Layout



Chapter 4

Schematic and Bill of Materials

The TPS54314EVM schematic and bill of materials are presented in this chapter.

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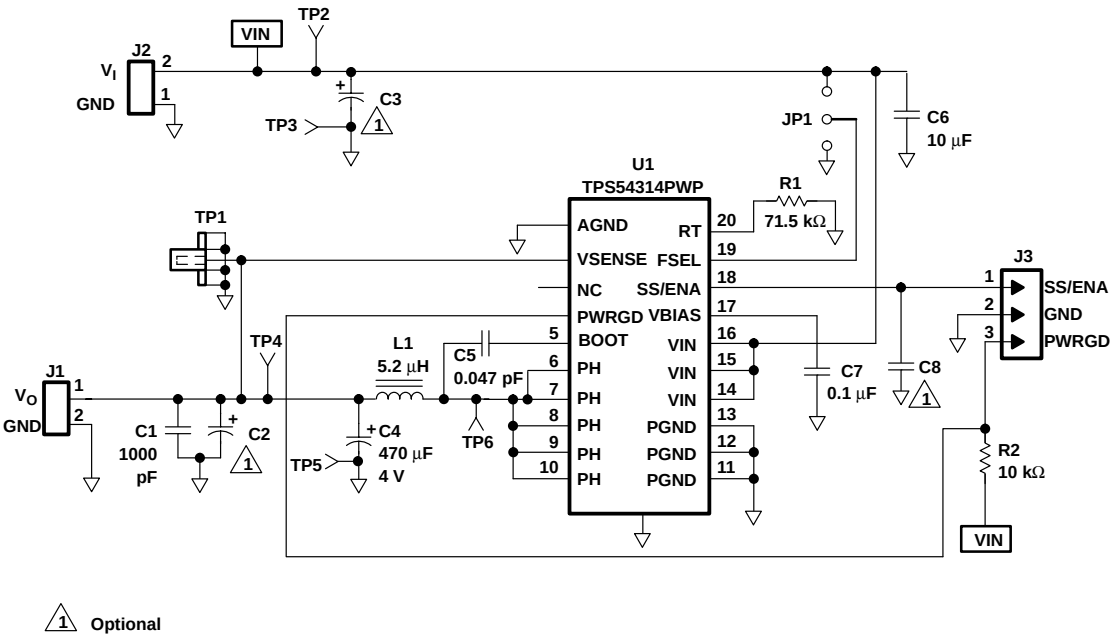
4.1 Schematic

Figure 4–1. TPS54314EVM Schematic



4.2 Bill of Materials

Table 4–1. TPS54314EVM Bill of Materials

Qty	Ref	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 1000 pF, 25 V, X7r, 10%	603	Murata	GRM39X7R102K25
2	C2, C3	Open	7343 (D)		
1	C4	Capacitor, POSCAP, 470 μF, 4 V, 40 mΩ, 20%	7343 (D)	Sanyo	4TPB470M
1	C5	Capacitor, ceramic, 0.047 μF, 25 V, X7R, 10%	603	Murata	GRM39X7R473K25
1	C6	Capacitor, ceramic, 10 μF, 10 V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	C7	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	603	Murata	GRM39X7R104K25
1	C8	Open	603		
2	J1, J2	Terminal block, 2 pin, 6 A, 3,5 mm	0.27 x 0.25	OST	ED1514
1	J3	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN
1	JP1	Header, 3 pin, 100 mil spacing, (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 5.2 μH, 5.5 A, 16 mΩ	0.405 sq	Sumida	CDRH104R–5R2
1	R1	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
1	R2	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Std
1	TP1	Adaptor, 3,5-mm probe clip (or 131-5031-00)	0.2	Tektronix	131-4244-00
3	TP2, TP4, TP6	Test point, red, 1 mm	0.038	Farnell	240–345
2	TP3, TP5	Test Point, Black, 1 mm	0.038	Farnell	240–333
1	U1	IC, IFET power controller, 1.8 V, 3 A	PWP20	TI	TPS54314PWP
1	—	PCB, 3″ x 3″ x 0.062″		Any	SLVP204
2	—	Shunt, 100-mil, black	0.100	3M	929950–00